REMARKS

Claims 1-18 are pending in the above-identified application. Claims 1-3, 8, 11 and 14 are amended. No claims are canceled or added.

The Examiner objected to the title of the invention in the specification. Applicants amend the title of the above-identified application. Please see Amendments to the Specification on page 2. Accordingly, withdrawal of the objection is now solicited.

The Examiner objected to claim 2 because of a grammatical informality. Applicants amend claim 2. Please see the Listing of Claims on page 3. Accordingly, withdrawal of the objection is now solicited.

The Examiner rejected claims 8, 11, and 14 under 35 U.S.C. 112, second paragraph, for insufficient antecedent basis for the limitation "the third hard mask". Applicants amend claims 8, 11, and 14. Please see Listing of Claims on page 3. Accordingly, withdrawal of the objection is now solicited.

The Examiner rejected claim 3 under 35 U.S.C. 112, second paragraph, as being indefinite. Applicants amend claim 3. Please see Listing of Claims on page 3. Support for this amendment is found on page 8 of the specification. Accordingly, withdrawal of the objection is now solicited.

The Examiner rejected claims 1-5 under 35 U.S.C. 102(e) as being anticipated by *Huang et al.* (2003/0119305). In order for a reference to be anticipatory under §102, it must detail the

claimed invention as it is set forth in the claim. Applicants amend claim 1. It is believed that the Listing of Claims on page 3 distinguishes over the prior art.

The invention described in claim 1 of the present invention defines that in a method for manufacturing a semiconductor device for forming a wiring by a dual damascene method, the method comprising the steps of: forming a mask (6) for a wiring trench patterned to be a wiring trenches pattern on an interlayer dielectric film (5) (see Figs. 1A to 1D); forming a mask (10) for a via hole patterned to be a via holes pattern on the mask (6) for the wiring trench by using a multilayered resist (see Figs. 1E and 1F); forming a hole shallower than a thickness of the interlayer dielectric film (5) in the interlayer dielectric film (5) by processing the interlayer dielectric film (5), using the mask (10) for the via hole (see Figs. 1g to 1i); forming a wiring trench in the interlayer dielectric film (5) by processing the interlayer dielectric film (5), using the mask (6) for the wiring trench, and simultaneously forming a via hole by passing the hole through a base layer (see Figs. 1j to 1m); and embedding a wiring material (14) in the wiring trench and the via hole (see Figs. 1N and 1O).

Huang discloses that, after mask films 58, 59 and 60 for wiring trenches are stacked, mask films 61 and 62 for via holes are formed without patterning of the mask films 58, 59 and 60 (see Fig. 15).

Accordingly, the present invention is not anticipated by *Huang* and should not be rejected under 35 U.S.C. § 102(e). The present invention discloses that the mask (10) for the via hole is formed on the mask (6) for the wiring trench patterned to be wiring trenches pattern, whereas

Huang discloses that the mask films 61 and 62 for via holes are formed without patterning of the mask films 58, 59 and 60.

As claims 2-18 depend from claim 1, they should likewise be allowable in light of the above comments in regard to the §102 rejection by nature of their dependency.

The Examiner rejected claims 6-10, 12-13 and 15-18 under 35 USC §103(a) as being unpatentable over *Huang* in view of *Takase et al.* (U.S. Patent Application No. 6,051,508). Claims 6-10, 12-13 and 15-18 are dependent on claim 1, and each claim has the limitation of the step of forming the mask (10) for the via hole on the mask (6) for the wiring trench patterned to be a wiring trenches pattern, as in claim 1.

Takase et al., on the other hand, discloses that, after forming a mask film 24 for a contact hole, a mask film 29 for a wiring trench is formed on the layer upper than the mask film 24 for the contact hole. Accordingly, withdrawal of the obviousness rejection is now solicited.

The Examiner rejected claims 16 and 18 under 35 U.S.C. 103(a) as being unpatentable over *Huang* in view of *Takase et al.* as applied to claims 1, 6, and 12, and further in view of *Pan et al.* (2004/0023497).

Pan et al. also fails to disclose the step of forming a mask for a via hole on the mask for the wiring trench patterned to be wiring trenches pattern as in the present invention. Accordingly, withdrawal of the obviousness rejection is solicited.

Applicant appreciates the indication that claims 11 and 14 would be allowable if rewritten to overcome the rejections under 35 USC §112, second paragraph, and to include all of the

limitations of the base claim and any intervening claims. However, for the reasons detailed above, it is believed that all claims are allowable.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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